VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Page 65, paragraph 4, lines 33-35, to page 66, paragraph 1, lines 2-8, amend as follows:

Transistors 818 and 820 form a cross-coupled pair that injects a current into tank #1 ~~that~~ in which the current through the transistor 818 is exactly 180 degrees out of phase with ~~V1~~ the current in the transistor 820. Likewise, transistors 822 and 824 form a cross-coupled pair that injects a current into tank #2 ~~that~~ in which the current through the transistor 822 is exactly 180 degrees out of phase with ~~V2~~ the current in the transistor 824. The first set of coupling devices 834, 836 injects a current into tank ~~#2~~ #1 that is ~~in phase with V1~~ 90 degrees out of phase with the current injected respectively by the transistors 818, 820. The second set of coupling devices 838, 840 injects a current into tank ~~#1~~ #2 that is ~~in phase with V2~~ 90 degrees out of phase with the current injected respectively by the transistors 822, 824. The tank impedances causes a frequency dependent phase shift. By varying the amplitude of the coupled signals, the frequency of oscillation changes until the phase shift through the tanks results in a steady-state solution. Varying the bias of the current source controls the gm of the coupling devices. Current sources 812, 816 provide control of VCO tuning. Current sources 810, 814 provide segmentation of the VCO tuning range.

Page 72, paragraph 4, lines 25-35, to page 73, paragraph 1, lines 2-4, amend to read as follows:

With an input dynamic range of 50 dB, the RSSI circuit is designed to detect the levels of rejection provided by the polyphase filtering. The outputs of RSSI block 284 and RSSI block 285 are coupled to a comparator 280 where the level of signal rejection of each polyphase filter is compared by comparator 280. The outputs of

the RSSI blocks are also coupled to the control logic 286. The control logic 286 determines from the RSSI outputs which polyphase filter has a lower amount of signal suppression. Then, the control logic 286 adjusts the frequency tuning of that filter in an incremental step via the control logic 286. This is done by either increasing the tuned frequency of the first filter (polyphase A) filter 280, or by decreasing the tuned frequency of the second filter (polyphase B) 282 by changing the appropriate 4-bit control word. This process continues in successive steps until the 4-bit control word in each branch are identical, at which point, the RC values of the two polyphase filters are equal. ~~This results in a change of state of the comparator 288 output. The change in state of the comparator output disables the control logic 286 locking up the 4-bit control word for optimum calibration of the RC circuits in the transmitter, receiver and LO generator.~~ The 4-bit control word provides a maximum deviation of only $\pm$5%.

In the Claims:

~~113~~. (Amended) The adaptive transceiver of claim ~~121~~ 112 further comprising means for amplifying the received first signal, and means for programming gain of the amplifying means.

~~114~~. (Amended) The adaptive transceiver of claim ~~121~~ 112 wherein the downconverting means downconverts the received first signal to an intermediate frequency signal.

~~115~~. (Amended) The adaptive transceiver of claim ~~123~~ 114 further comprising means for filtering the intermediate frequency signal, and means for programming a frequency band of the filtering means.

116. (Amended) The adaptive transceiver of claim ~~123~~ 114 further comprising means for downconverting the intermediate frequency signal to a baseband signal.

117. (Amended) The adaptive transceiver of claim ~~125~~ 116 further comprising means for demodulating the baseband signal, and means programming demodulation for the demodulation means.

118. (Amended) The adaptive transceiver of claim ~~121~~ 112 wherein the clock frequency programming means comprises means for mixing a second clock with a third clock.

119. (Amended) The adaptive transceiver of claim ~~127~~ 118 wherein the clock frequency programming means further comprises means for generating the third clock by dividing the second clock by an integer N.

120. (Amended) The adaptive transceiver of claim ~~128~~ 119 wherein the clock frequency f_{LO} is equal to f_{VCO} (N+1) / N, wherein f_{VCO} equals a frequency of the second clock.

121. (Amended) The adaptive transceiver of claim ~~129~~ 120 wherein N = 2.

122. (Amended) The adaptive transceiver of claim ~~121~~ 112 further comprising means for amplifying the upconverted first signal before transmitting the upconverted first signal into space, and means for programming gain of the amplifying means.

123. (Amended) The adaptive transceiver of claim ~~121~~ 112 further comprising means for filtering the first signal, and means for programming a frequency band of the filtering means.

124. (Amended) The adaptive transceiver of claim ~~121~~ 112 wherein the transmitting and receiving means each have a component, the adaptive transceiver further comprising means for calibrating one of the components of the transmitting and receiving means.

125. (Amended) The adaptive transceiver of claim ~~131~~ 124 wherein one of the components comprises a resistor.

126. (Amended) The adaptive transceiver of claim ~~131~~ 124 wherein one of the components comprises a capacitor.

127. (Amended) The adaptive transceiver of claim ~~131~~ 124 wherein the calibrating means is configured to calibrate the component of the transmitting means.

128. (Amended) The adaptive transceiver of claim ~~131~~ 124 wherein the calibrating means is configured to calibrate the component of the receiving means.

129. (Amended) The adaptive transceiver of claim ~~131~~ 124 further comprising means for testing one of the receiving and transmitting means by coupling test data thereto and monitoring an output thereof.

131. (Amended) The integrated circuit of claim ~~137~~ 130 wherein the receiver component comprises a filter having a programmable frequency band.

132. (Amended) The integrated circuit of claim ~~137~~ 130 wherein the receiver component comprises an amplifier having a programmable gain.

133. (Amended) The integrated circuit of claim ~~137~~ 130 wherein the receiver component comprises a demodulator with programmable demodulation.

134. (Amended) The integrated circuit of claim ~~137~~ 130 wherein the receiver component comprises an amplifier having a programmable gain, and the receiver further comprises a filter coupled to the amplifier and having a programmable frequency band, and a demodulator coupled to the filter and having programmable demodulation.

135. (Amended) The integrated circuit of claim ~~137~~ 130 wherein the transmitter component comprises a filter having a programmable frequency band.

136. (Amended) The integrated circuit of claim ~~137~~ 130 wherein the transmitter component comprises an amplifier having a programmable gain.

137. (Amended) The integrated circuit of claim ~~137~~ 130 wherein the transmitter component comprises a filter having a programmable frequency band, and an amplifier coupled to the filter and having a programmable gain.

138. (Amended) The integrated circuit of claim ~~144~~ 137 wherein the receiver component comprises a second amplifier having a programmable gain, and the receiver further comprises a second filter coupled to the second amplifier and having a programmable frequency band, and a demodulator coupled to the second filter and having programmable demodulation.

139. (Amended) The integrated circuit of claim ~~137~~ 130 further comprising an local oscillator coupled to the receiver and transmitter.

140. (Amended) The integrated circuit of claim ~~146~~ 139 wherein the local oscillator comprises a clock generator which outputs a clock to the receiver and transmitter.

141. (Amended) The integrated circuit of claim ~~147~~ 140 wherein the transmitter comprises a mixer to mix the clock with a baseband signal.

142. (Amended) The integrated circuit of claim ~~148~~ 141 wherein the transmitter further comprises an amplifier coupled to the mixer, the amplifier being the programmable transmitter component.

143. (Amended) The integrated circuit of claim ~~148~~ 141 wherein the transmitter further comprises a filter coupled to the mixer, the filter being the programmable transmitter component.

144. (Amended) The integrated circuit of claim ~~147~~ 140 wherein the transmitter component comprises a filter with a programmable frequency band to filter a baseband signal, and wherein the transmitter further comprises a mixer coupled to the filter to mix the clock with the filtered baseband signal, and an amplifier coupled to the mixer and having a programmable gain.

145. (Amended) The integrated circuit of claim ~~147~~ 140 wherein the receiver comprises a mixer to mix the clock with a received signal from a wireless source.

146. (Amended) The integrated circuit of claim ~~152~~ 145 wherein the receiver further comprises an amplifier coupled to the mixer, the amplifier being the programmable receiver component.

147. (Amended) The integrated circuit of claim ~~152~~ 145 wherein the receiver further comprises a filter coupled to the mixer, the filter being the programmable receiver component.

148. (Amended) The integrated circuit of claim ~~152~~ 145 wherein the receiver further comprises a demodulator coupled to the mixer, the demodulator being the programmable receiver component.

149. (Amended) The integrated circuit of claim ~~147~~ 140 wherein the receiver component comprises an amplifier having a programmable gain to amplify a received signal from an external wireless source, and wherein the receiver further comprises a first mixer coupled to the amplifier to mix the amplified received signal with the clock, a filter coupled to the first mixer and having a programmable frequency band, a second mixer coupled to the filter, and a demodulator coupled to the filter and having programmable demodulation.

150. (Amended) The integrated circuit of claim ~~156~~ 149 wherein the transmitter component comprises a second filter with a programmable frequency band to filter a baseband signal, and wherein the transmitter further comprises a third mixer coupled to the second filter to mix the clock with the filtered baseband signal, and a second amplifier coupled to the third mixer and having a programmable gain.

151. (Amended) The integrated circuit of claim ~~147~~ 140 wherein the local oscillator comprises a second clock generator which outputs a second clock to the receiver.

152. (Amended) The integrated circuit of claim ~~158~~ 151 wherein the second clock generator comprises an oscillator and a divider coupled to the oscillator, the divider having a control input coupled to the controller to program a frequency of the second clock.

153. (Amended) The integrated circuit of claim ~~147~~ 140 wherein the clock generator comprises a voltage controlled oscillator to generate the clock, the voltage controlled oscillator a having frequency different than a frequency of the clock.

154. (Amended) The integrated circuit of claim ~~160~~ 153 wherein the clock generator further comprises a divider coupled to the voltage controlled oscillator, and a mixer coupled to both the divider and the voltage controlled oscillator, the mixer having an output comprising the clock to the transmitter and receiver.

155. (Amended) The integrated circuit of claim ~~161~~ 154 wherein the divider further comprises a control input coupled to the controller to program the frequency of the clock.

156. (Amended) The integrated circuit of claim ~~161~~ 154 wherein the clock generator further comprises a phase lock loop comprising the voltage controlled oscillator, the phase lock loop having a control input coupled to the controller to program the frequency of the voltage controlled oscillator.

157. (Amended) The integrated circuit of claim ~~137~~ 130 wherein the transmitter and receiver each have a second component, and the controller is configured to calibrate one of the transmitter and receiver second components.

158. (Amended) The integrated circuit of claim ~~164~~ 157 wherein the second component comprises a resistor.

159. (Amended) The integrated circuit of claim ~~164~~ 157 wherein the second component comprises a capacitor.

160. (Amended) The integrated circuit of claim ~~164~~ 157 wherein the controller is configured to calibrate the transmitter second component.

161. (Amended) The integrated circuit of claim ~~164~~ 157 wherein the controller is configured to calibrate the receiver second component.

162. (Amended) The integrated circuit of claim ~~164~~ 157 wherein the controller is configured to calibrate both the receiver and transmitter second components.

163. (Amended) The integrated circuit of claim ~~164~~ 157 further comprising a self testing unit coupled to the receiver and transmitter, the self testing unit being configured to coupled test data to one of the receiver and transmitter, and monitor an output thereof.